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CERTIFICATE OF TRANSMISSION

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I hereby certify that the following correspondence is being facsimile transmitted to the attention of the Director of the US Patent and Trademark Office on the above date via the following facsimile number: **571-273-8300.**

Replacement Declaration (2 sheets)
Replacement Declaration Under 37 C.F.R. § 1.132 (9 sheets)

Application Number	09/697,419	Art Unit:	2124
Confirmation No.:	5374	Examiner:	Vu, Tuan A.
Filing Date:	26 October 2000	Inventor:	McNutt, Alan

Document Submission Date: 19 August 2005

Docket: 1999P07938US01 (1009-045) **Pages: 12**

19 Aug 2005	Eden Brown	Eden Brown
Date	Name of Certifier	Signature of Certifier

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PATENT

Application # 09/697,419

Attorney Docket # 1999P07938US01 (1009-045)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Alan D. McNutt
Application #	:	09/697,419
Confirmation #	:	5374
Filed	:	26 October 2000
Application Title	:	RE-PROGRAMMABLE FLASH MEMORY MICRO CONTROLLER AS PROGRAMMABLE LOGIC CONTROLLER
Art Unit #	:	2124
Latest Examiner	:	Tuan A. Vu

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLACEMENT DECLARATION

Please replace the Declaration Under 37 C.F.R. § 1.132 of Dr. Ronald D. Williams filed on 2 May 2005 with the attached Declaration Under 37 C.F.R. § 1.132 of Dr. Ronald D. Williams, which corrects each mention of the priority date of the application to 26 October 1999.

PATENT

Application # 09/697,419

Attorney Docket # 1999P07938US01 (1009-045)

CONCLUSION

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Deposit Account No. 50-2504. The Examiner is invited to contact the undersigned at 434-972-9988 to discuss any matter regarding this application.

Respectfully submitted,

Michael Haynes PLC

Michael N. Haynes

Date: 19 August 2005

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AMENDMENT UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2124
PATENT
ATTORNEY DOCKET NO. 1999P07938US01 (1009-045)
SERIAL NO. 09/697,419

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Alan D. McNutt
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Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLACEMENT DECLARATION UNDER 37 C.F.R. § 1.132

Sir:

I, Dr. Ronald D. Williams, a citizen of the United States, whose full post office address is 1715 Hearthglow Lane, Charlottesville, VA 22901 declare as follows under penalty of perjury.

Background

1. I hold a Ph.D. degree in Electrical Engineering from the Massachusetts Institute of Technology awarded in 1984.
2. I hold a M.S. degree in Electrical Engineering from the University of Virginia

awarded in 1978.

3. I hold a B.S. degree in Electrical Engineering from the University of Virginia awarded in 1977.
4. I am currently an associate professor of Electrical & Computer Engineering at the University of Virginia.
5. Since 1984, I have worked continually in the field of electrical engineering with particular emphasis in embedded computing with applications in control and signal processing.
6. During my career, I have been granted five U.S. patents for my own inventions in the field of embedded computing.

Review

7. I have reviewed Application Serial No. 09/697,419 (hereinafter the present application).
8. I have reviewed the USPTO Office Action dated 4 January 2005 (hereinafter the "Office Action") regarding Application Serial No. 09/697,419.
9. I have reviewed U.S. Patent No. 5,519,843 (Moran) and U.S. Patent No. 6,263,487 (Stripf).
10. Among the devices with which I was familiar prior to 26 October 1999, the priority

date of Application Serial No. 09/697,419, were devices of the type recited in Moran and Stripf.

Moran Uses Three Chips

11. Each of independent claims 4, 5, 7, 9, and 11 recite **"a single chip program execution device"** "lacking a memory device external to said single chip program execution device."

12. One skilled in the art as of 26 October 1999, the priority date of the present application would not have found that Moran expressly or inherently teaches or suggests "a single chip program execution device" "lacking a memory device external to said single chip program execution device."

13. Instead, one skilled in the art would have found that Moran allegedly recites a "FIG. 1 is a block diagram of a conventional computer system; FIG. 2 is a block diagram of an exemplary system according to the present invention; FIG. 3 is a block diagram of a flash memory device according to the present invention." See col. 2, lines 39-42. In describing these drawings, Moran allegedly contrasts FIG. 2 from FIG. 1 by reciting "the ROM BIOS chip is replaced by a **flash memory system chip** ... Such a system is shown by the block diagram of FIG. 2, wherein the flash memory system 20 replaces the ROM BIOS chip 14 ... As seen in FIG. 3, flash memory systems ... comprise ... A flash memory device 30 provides the storage capability for the

integrated circuit package and a controller 32 provides logic functions which are used to interface the flash memory device 30 with the rest of the system via the system bus." See col. 3, lines 2-21. The only operative embodiment presented by Moran in FIG. 2 clearly illustrates a system that Moran alleged teaching is limited to 3 chips, namely **a "CPU" chip** and **a "RAM" chip** in communication with **a separate "IC" chip**.

14. The Office Action characterizes Moran's FIG. 5 as supporting statements such as "Fig. 5 – controller with system memory 12 comprising flashed BIOS and separated and executing independent from any external memory reads on lacking a memory device external to said execution device." See page 8.

15. The statement of the Office Action in paragraph 28 is factually incorrect from the point of view of one skilled in the art as of 26 October 1999, the priority date of the present application. One skilled in the art would have not have found that Moran expressly or inherently teaches or suggests "a single chip program execution device" "lacking a memory device external to said single chip program execution device."

16. One skilled in the art would have found Moran to allegedly recite "FIG. 5 illustrates windows opened between a flash memory device and system memory according to the present invention". *See* Col. 2, lines 45-48. Moran further allegedly recites that "the term 'window' is used to refer to a memory mapping scheme between the flash

memory device 30 and the system memory 12." See col. 3, lines 39-41.

17. Thus, one skilled in the art would have found that regarding FIG. 5 Moran allegedly maps memory between two devices on separate chips controlled by an execution device (CPU) on a third chip. *See*, FIG. 2; *see also*, col. 3, lines 37-49.

18. Thus, one skilled in the art would not have found that Moran expressly or inherently teaches or discloses "a single chip program execution device" "lacking a memory device external to said single chip program execution device."

Moran Does Not Teach or Suggest a Programmable Logic Controller

19. Each of pending claims 4-11 of the present application recite a "programmable logic controller."

20. The Office Action recites "Moran discloses a **programmable controller** (Fig. 9)." See Page 3.

21. The Office Action further recites "an integrated controller (see Fig. 9) and the use of code to emulate more than one type of devices (see col.7, lines 14-23) wherein a programmable memory stores user programs for effecting logic to implement the control over an OS and related functionalities as taught by Moran (see SUMMARY) **suggests a form of programmable logic controller**, and the concept of emulation/simulation of multiple devices requiring control is suggested." See Page 4.

22. One skilled in the art would find the statements of the Office Action recited in paragraph 12 and paragraph 13 factually incorrect as of 26 October 1999, the priority date of the present Application.

23. In construing the claims of the present application, one skilled in the art as of 26 October 1999, the priority date of the present application, would have looked to a reference source such as Webster's online dictionary for a definition of the term "programmable logic controller." Webster's defines a programmable logic controller as a "device used to automate monitoring and control of [an] industrial plant." *Available at*, http://www.websters-online-dictionary.org/definition/programmable+logic+controller (definition dated 2/11/1997).

24. One skilled in the art would not have found that Moran expressly or inherently teaches or recites a "programmable logic controller."

25. Instead, one skilled in the art would have found that Moran allegedly recites "FIG. 9 is a pin diagram of an **integrated circuit** package according to the present invention." See col. 2, lines 55-56.

26. One skilled in the art would not have found the **"integrated circuit** package" allegedly recited by Moran to expressly or inherently teach or recite a **"programmable logic controller."**

Moran Does Not Teach or Suggest Programmable Logic Controller I/O functions

27. Pending claim 4 of the present application recites a "**programmable logic controller I/O functions.**"

28. The Office Action recites "in view of Moran's teachings as to be able to initialize the power settings or memory input/output resetting of the controller ... such kernel related support instructions as well as **input/output routines or I/O functions are strongly implied if not disclosed.**" See page 4.

29. One skilled in the art would have found the statements of the Office Action recited in paragraph 20 factually incorrect as of 26 October 1999, the priority date of the present application.

30. Instead, one skilled in the art would have construed the term "programmable logic controller" to have the definition provided in paragraph 15.

31. One skilled in the art would have found that Moran allegedly recites at "power-on, the controller performs a reset and opens a window as a 64 KB window into the BIOS stored in block 1 of the flash memory device 30". See col. 4, lines 16-18.

32. One skilled in the art would not have equated activities internal to Moran's "integrated circuit" at "power-on" to expressly or inherently teach or suggest "**programmable logic controller I/O functions.**"

Placing a Single Chip Program Execution Device in Stripf Would Render Stripf Inoperative

33. One skilled in the art as of 26 October 1999, the priority date of Application Serial No. 09/697,419 would not have attempted to place a single chip program execution device in Stripf.

34. One skilled in the art would have found that Stripf allegedly recites that a "programmable controller is described in Siemens Catalog ST 70, 1995. With a programming unit, a user creates a program for controlling an industrial process, including software function blocks, e.g., in the form of organization blocks, program blocks and entity data blocks." Col. 1, lines 10-15.

35. One skilled in the art would have found that Stripf allegedly recites an "important requirement of a programmable controller [element 6, labeled "PLC" in FIG. 1] is that a control program formed by multiple software function blocks must be able to run cyclically and/or with interrupt control during control operation. These software function blocks must be designed so that they are loadable and can be tied into the control program while it is running." See col. 2, lines 9-20.

36. Each of independent claims 4, 5, 7, 9, and 11 recite "a single chip program execution device" that comprises a "user program" and a "system support kernel" compiled together.

37. Even if Moran taught or suggested the elements recited in paragraph 35, by executing the claimed compilation of a "user program" and a "system support kernel" in Stripf's "programmable controller", one skilled in the art would have found no need or possibility of loading or tying Stripf's "software function blocks" "into the control program while it is running".

38. Thus, even if Moran disclosed the claim limitations asserted in the Office Action, an incorrect factual premise, attempting to place a "a single chip program execution device" that comprises a "user program" and a "system support kernel" compiled together in Stripf would cause Stripf's programmable logic controller to cease functioning according to the "requirements" disclosed therein.

I further declare that all statements made herein of my own knowledge are true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 18th day of August 2005

Dr. Ronald D. Williams